WHAT IS CLAIMED IS:

1. A semiconductor device which allows one electrically erasable and programmable nonvolatile memory cell to store multi-valued information therein, comprising:

a sense latch having a pair of input/output terminals;

bit lines provided in association with the respective input/output terminals of the sense latch;

a plurality of nonvolatile memory cells selectively connected to the bit lines and capable of electrically performing erasure and writing;

data latches respectively connected to the bit lines;

a first logic combining circuit connected to the data latches and the sense latch; and

a control circuit connected to the sense latch, the data latches and the first logic combining circuit;

wherein the first logic combining circuit generates control data used to define to which threshold voltage state a threshold voltage state of one nonvolatile memory cell is set, every plural bits of write data and to supply the generated data to the corresponding sense latch and data latches respectively on a parallel basis, and

wherein the control circuit is capable of

performing program control so as to control the operations of the sense latch, the data latches and the first logic combining circuit to thereby bring each volatile memory cell to a predetermined threshold voltage state according to a logic value of the control data supplied from the first logic combining circuit to the sense latch and successively bring volatile memory cells to predetermined threshold voltage states according to logic values of control data supplied from the data latches to the sense latch.

2. A semiconductor device comprising:

a first latch having a pair of input/output nodes;

a first bit line connected to one input/output node of the first latch and connected with a plurality of electrically rewritable nonvolatile memory cells;

a second bit line connected to the other input/output node of the first latch and connected with a plurality of electrically rewritable nonvolatile memory cells;

a second latch connected to the first bit line;

a third latch connected to the second bit line;

a first logic combining circuit connected to the first through third latches;

a second logic combining circuit connected to the first bit line;

a third logic combining circuit connected to the

second bit line; and

a control circuit connected to the first through third latches and the first through third logic combining circuits;

wherein the first logic combining circuit generates control data used to define to which of first through third threshold voltage states one nonvolatile memory cell is set with respect to a fourth threshold voltage state and to supply the generated data to the corresponding first through third latches, and

wherein the control circuit is capable of performing program control so as to control the operations of the first through third latches and the first through third logic combining circuits to thereby bring each volatile memory cell to a first threshold voltage state according to a logic value of the control data supplied from the first logic combining circuit to the first latch, bring each volatile memory cell to a second threshold voltage state according to a logic value of the control data supplied from the second latch to the first latch, and bring each volatile memory cell to a third threshold voltage state according to a logic value of the control data supplied from the third latch to the first latch.

3. The semiconductor device according to claim 2, wherein the control circuit determines whether the

threshold voltage state of the corresponding nonvolatile memory cell has reached an intended threshold voltage state through the use of the second and third logic combining circuits each time a voltage is applied for varying the threshold voltage of each nonvolatile memory cell in response to the predetermined logic value of the control data supplied to the first latch under the program control, and inverts the logic value of the control data of the first latch when the threshold voltage state thereof is found to have reached the intended threshold voltage state and subsequently suppresses a change in threshold voltage state with respect to the corresponding nonvolatile memory cell.

4. The semiconductor device according to claim 3, wherein the control circuit is capable of performing disturb check control for determining under the program control whether the threshold voltage state of the nonvolatile memory cell to be maintained at the fourth threshold voltage state is distinguishable from an adjacent threshold voltage state higher than that in threshold voltage, first erratic check control for determining under the program control whether a threshold voltage state of a nonvolatile memory cell, which is to be changed to the adjacent threshold voltage state, is distinguishable from a further adjacent threshold voltage state higher than that in threshold voltage, and second

erratic check control for determining under the program control whether a threshold voltage state of a nonvolatile memory cell, which is to be changed to the further adjacent threshold voltage state, is distinguishable from a still further adjacent threshold voltage state higher than that in threshold voltage.

5. The semiconductor device according to claim 4, wherein the disturb check control is a process for allowing the control circuit to determine through the use of the second and third logic combining circuits whether each memory cell should be maintained at the fourth threshold voltage state, based on the control data held in the second and third latches and data read from the corresponding memory cell, and for allowing the control circuit to set control data having a predetermined logic value prior to the logic value inversion to the first latch only with respect to the memory cell to be held in the fourth threshold voltage state thereby to determine whether the threshold voltage state of the memory cell is distinguishable from the adjacent threshold voltage state higher than that in threshold voltage.

6. The semiconductor device according to claim 5, wherein the first erratic check control is a process for allowing the control circuit to transfer the control data held in a predetermined one of the second latch and the

third latch to the first latch through the use of the second and third logic combining circuits thereby to determine whether the threshold voltage state of the memory cell is distinguishable from the further adjacent threshold voltage state higher than that in threshold voltage, and

the second erratic check control is a process for allowing the control circuit to transfer the control data held in the predetermined other of the second latch and the third latch to the first latch through the use of the second and third logic combining circuits thereby to determine whether the threshold voltage state of the memory cell is distinguishable from the further adjacent threshold voltage state higher than that in threshold voltage.

7. The semiconductor device according to any one of claims 4 through 6, wherein when a state undistinguishable from a predetermined threshold voltage state is detected upon the disturb check control, the first erratic check control or the second erratic check control, the control circuit restores the control data sent from the first logic combining circuit to the first latch related to a memory cell, based on the control data held in the second and third latches and data read from the memory cell through the use of the second and third logic combining circuits, thereby allowing the resumption

of the program process.

8. The semiconductor device according to claim 7, wherein when the program process is resumed, each nonvolatile memory cell intended for the program process is the same as the immediately preceding program process.

9. The semiconductor device according to claim 7, wherein when the program process is resumed, each nonvolatile memory cell intended for the program process is a newly-specified one.

10. The semiconductor device according to any one of claims 4 through 6, wherein when a state undistinguishable from a predetermined threshold voltage state is detected upon the disturb check control, the first erratic check control or the second erratic check control, the control circuit restores the control data sent from the first logic combining circuit to the first latch related to a memory cell, based on the control data held in the second and third latches and data read from the memory cell through the use of the second and third logic combining circuits, and restores write data represented in 2-bit units, based on the restored latched data of the first latch circuit and the latched data of the second and third latches, thereby allowing the output of the restored write data to the outside through the

second and third latches.

11. A data processing system comprising:

a semiconductor device according to any one of claims 1 through 10;

a memory controller which access-controls the semiconductor device; and

a processor which controls the memory controller.

12. A memory card comprising:

a card substrate including,

a semiconductor device according to any one of claims 1 through 10, a memory controller which access-controls the semiconductor device, and an external interface circuit connected to the memory controller, all of which are packaged thereon.

13. A data processing system comprising:

a control device; and

one or plural nonvolatile memory devices connected to the control device;

wherein each of the nonvolatile memory devices has a first latch device connected to one ends of first and second bit lines, second and third latch devices respectively connected to the other ends of the first and second bit lines, and a plurality of memory cells respectively connected to the first and second bit lines,

wherein each of the memory cells is capable of changing a threshold voltage thereof so as to store predetermined data therein,

wherein a first control circuit is connected to the first through third latch devices, and generates threshold voltage information to be set to the memory cell and sets predetermined information to the first through the third latch devices according to the threshold voltage to be set to the memory cell,

wherein a second control circuit is provided which controls the setting of the threshold voltage to the memory cell according to control information from the control device, and

wherein the control device supplies the control information and the data to be stored in the memory cell to each of the nonvolatile memory devices and performs a predetermined control operation.

14. The data processing system according to claim 13, wherein the threshold voltage to be set to the memory cell has threshold voltage levels of three stages or more corresponding to information of at least 2 bits of the data to be stored in the memory cell.

15. The data processing system according to claim 14, wherein the nonvolatile memory device has a plurality of select lines,

the memory cells are respectively connected to the corresponding select lines, and

the change in threshold voltage of the memory cell is effected on a memory cell selected by the select line.

16. A data processing system comprising:

a control device; and

one or plural nonvolatile memory devices connected to the control device,

wherein the control device supplies control information and data to be stored in each of the nonvolatile memory devices to the one or plural nonvolatile memory devices or performs predetermined processing,

wherein the nonvolatile memory device has a control circuit and a plurality of bit lines, said bit lines being connected to a plurality of memory cells and information storage circuits, and said each memory cell having threshold voltage distributions of at least three stages and set to any of the threshold voltage distributions, based on information stored in the information storage circuit,

wherein the control circuit divides the data into at least partial data set by 2 bits, generates control information for determining the threshold voltage distribution of each memory cell, based on the partial data, and supplies the generated control information to

17. A nonvolatile memory device comprising:

a control circuit;

a data terminal;

a plurality of latch circuits;

a plurality of nonvolatile memory cells;

a plurality of word lines; and

a first decode circuit,

wherein each of said memory cells couples to corresponding word line, couples to corresponding latch circuit and is capable of having a threshold voltage within one of threshold voltage ranges,

wherein said first decode circuit decodes data, receives data having plurality bits from said data terminal and outputs a first signal to said latch circuit, and

wherein in a program operation, said control circuit controls to receiving data, to decoding data by said first decode circuit, to latching said first signal at said latch circuit coupled to memory cell objected to a first level programming, to supplying a program voltage to word line coupled to said memory cell after latching at said latch circuit, to latching said first signal at said latch circuit coupled to memory cell objected to a second level programming, and to supplying said program voltage to word line coupled to said memory cell after latching at said

latch circuit.

18. A nonvolatile memory device according to claim 17, further comprising a buffer circuit,

wherein said buffer circuit couples between said data terminal and said first decoder circuit for buffering data from said data terminal.

19. A nonvolatile memory device according to claim 18, further comprising a plurality of data lines,

wherein each of said data lines couples to corresponding memory cell and couples to corresponding latch circuit, and

wherein in said program operation, said latch circuit supplies a second signal to said memory cells during said supplying program voltage via said data line when said latch circuit is set said first signal

20. A nonvolatile memory device according to claim 19,

wherein in said program operation, said control circuit controls to supplying one voltage level ofverify voltages to said word line, to judging a threshold voltage level of memory cell which is supplied said second signal, and to supplying said program voltage to said word line and

supplying said second voltage to memory cell said threshold voltage of which has not been reached a preliminary voltage level corresponding to programming level, and

wherein each of said verify voltages is corresponding to one of threshold voltage ranges.

21. A nonvolatile memory device according to claim 20, further comprising a second decode circuit,

wherein said second decode circuit decodes address receiving from outside for selecting word line.

22. A nonvolatile memory device according to claim 21,

wherein one of said threshold voltage ranges is indicated an erase state and others of said threshold voltage ranges is indicated program states.

23. A nonvolatile memory device according to claim 22,

wherein in an erase operation, threshold voltage of memory cells coupled to said word line are moved into threshold voltage range indicated said erase state.